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PATENT & TRADEMARK OFFICE

Title: MULTI-LEVEL PULSE WIDTH MODULATION IN DIGITAL SYSTEM
Inventor Name: Ying Lau Lee
Appl. No. 10/678,614
Docket No.: HLEE-001XX

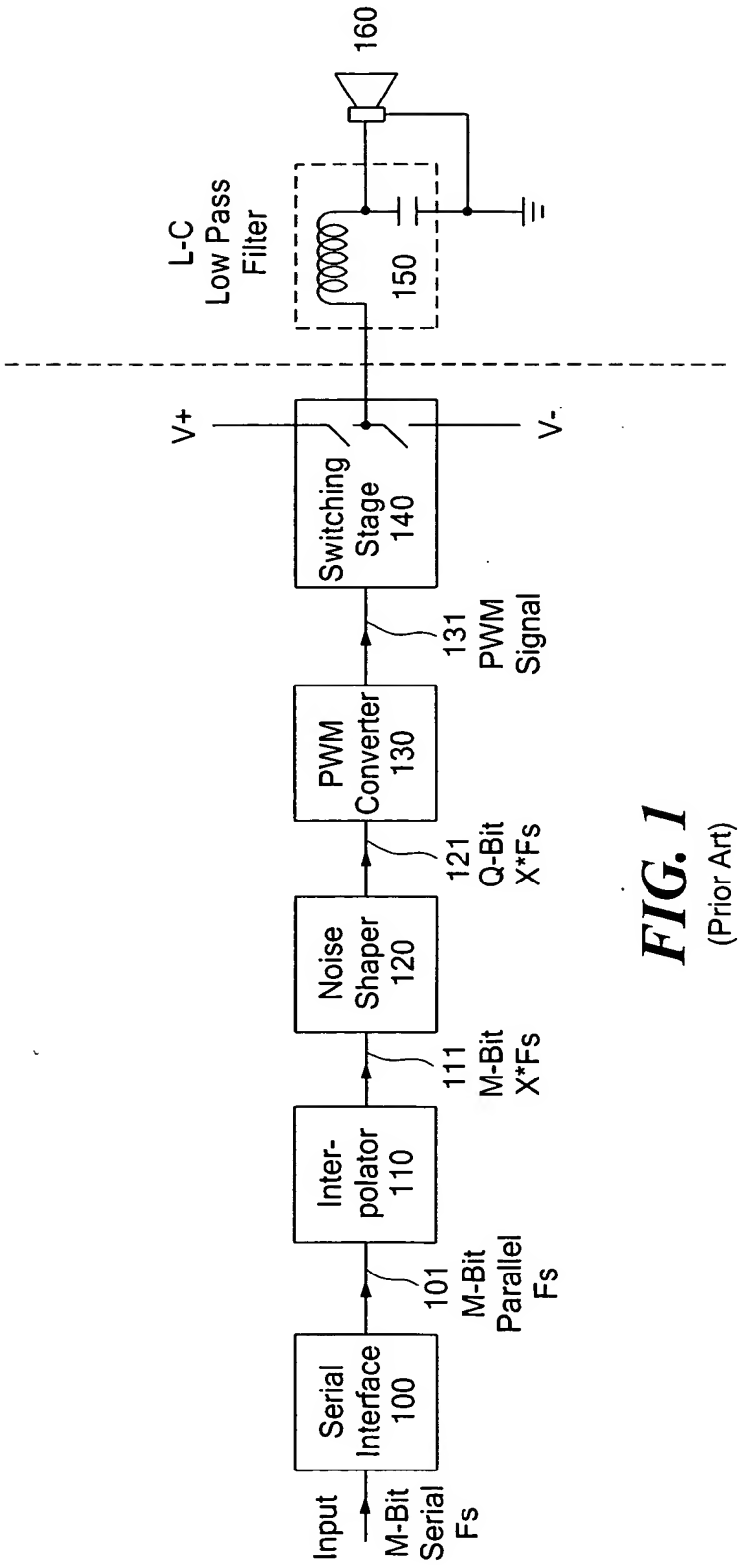

FIG. 1
(Prior Art)

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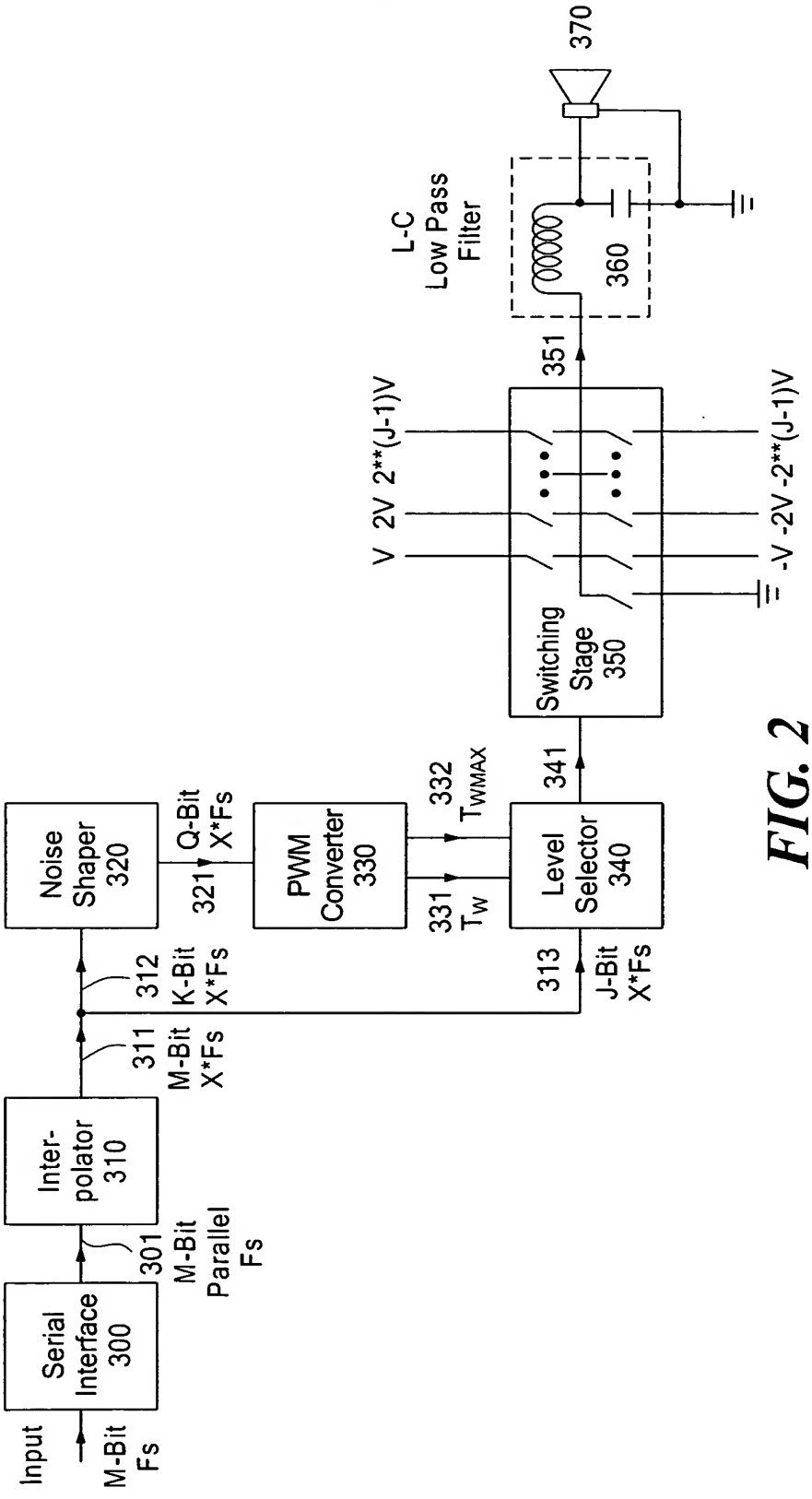

FIG. 2

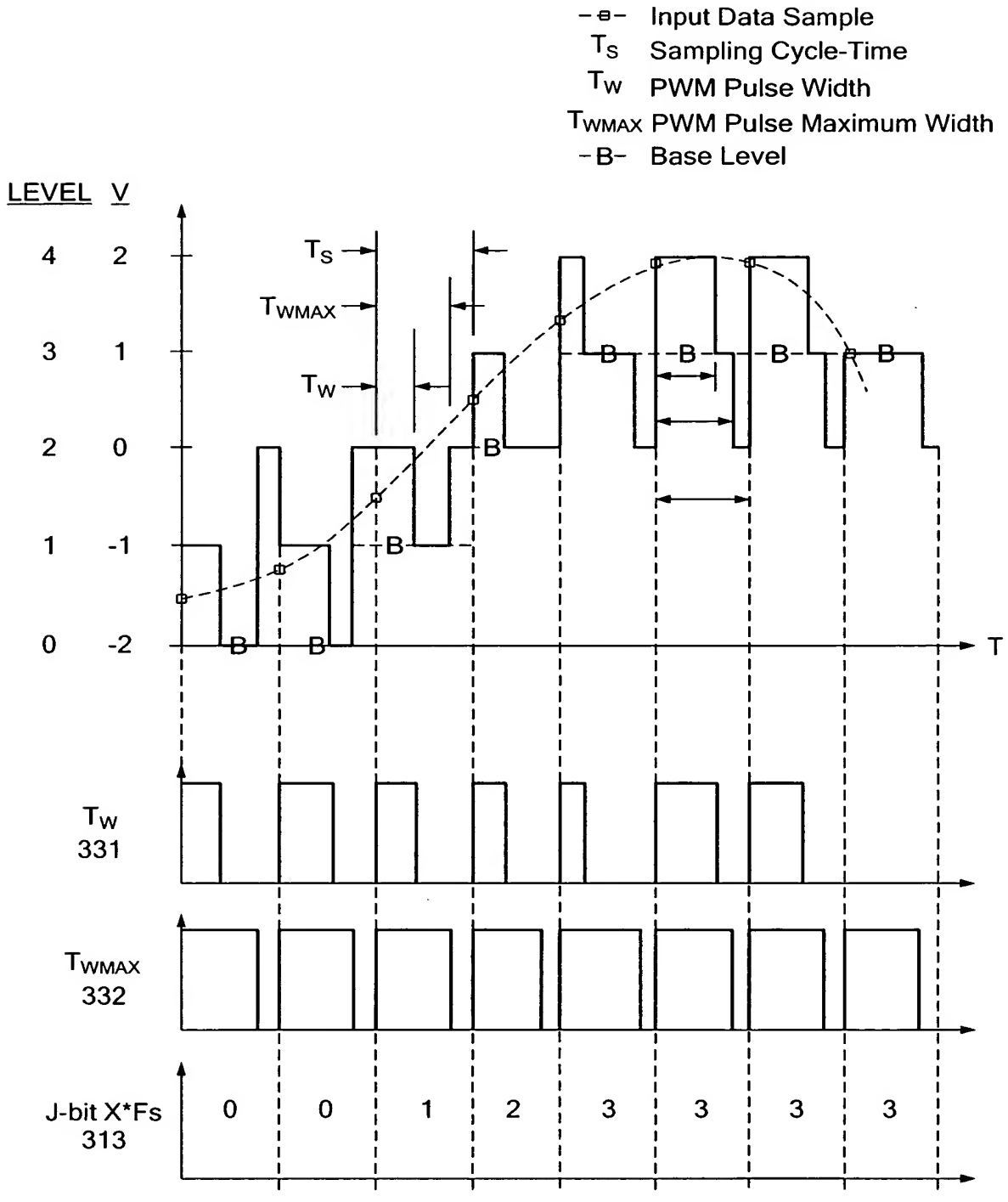
-e- Input Data Sample
Ts Sampling Cycle-Time
Tw PWM Pulse Width
TwMAX PWM Pulse Maximum Width
-B- Base Level
LEVEL V
4 2
3 1
2 0
1 -1
0 -2
Ts
TwMAX
Tw
B
T
Tw
331
TwMAX
332
J-bit X*Fs
313
0 0 1 2 3 3 3 3

FIG. 3

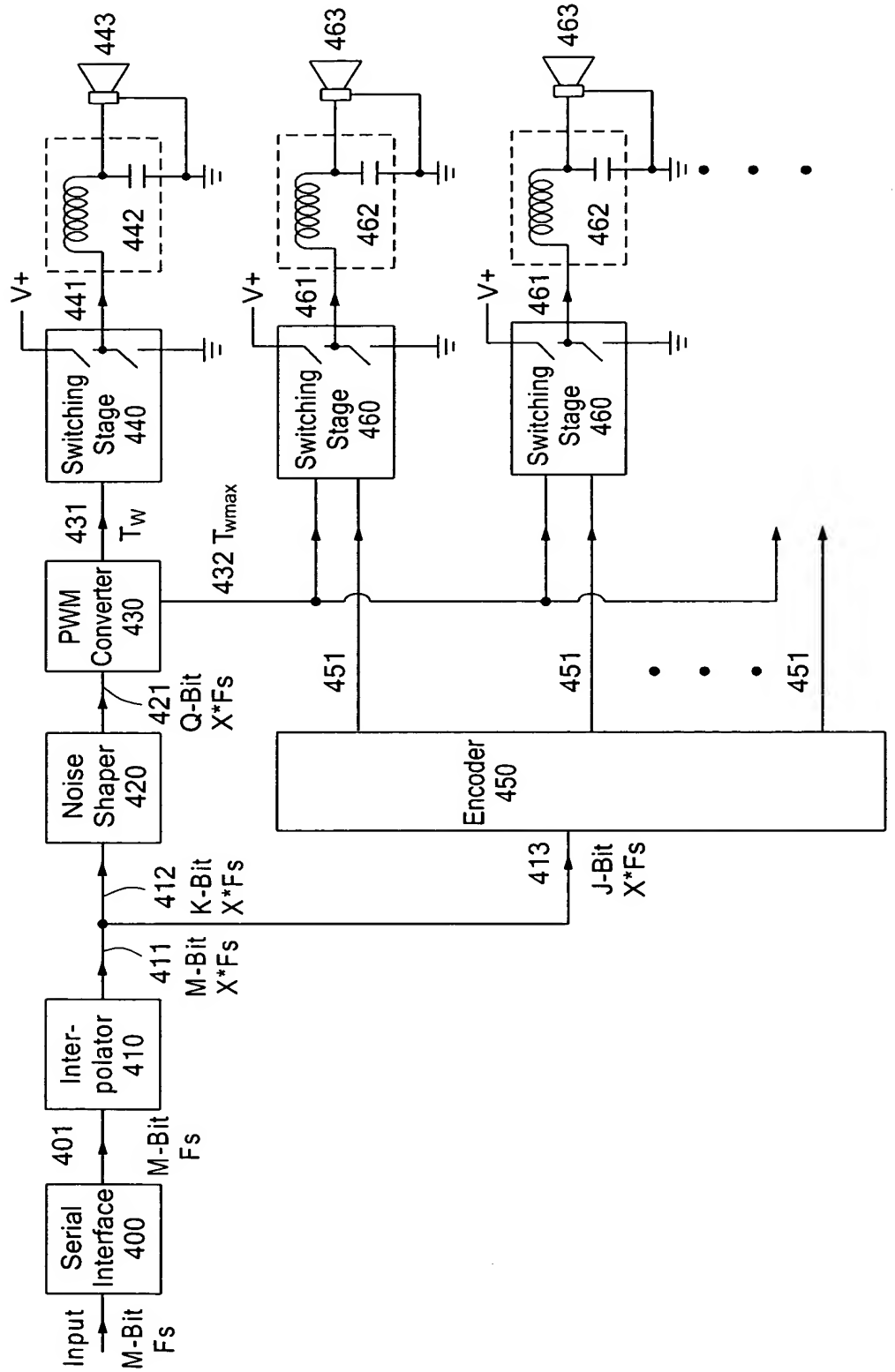
Input
M-Bit
Fs
Serial Interface 400
401
M-Bit
Fs
Inter-polator 410
411
M-Bit
X*Fs
412
K-Bit
X*Fs
Noise Shaper 420
421
Q-Bit
X*Fs
PWM Converter 430
431
T_w
432 T_{wmax}
Switching Stage 440
441
442
443
V+
Switching Stage 460
461
462
463
V+
Switching Stage 460
461
462
463
V+
451
451
451
Encoder 450
413
J-Bit
X*Fs

FIG. 4

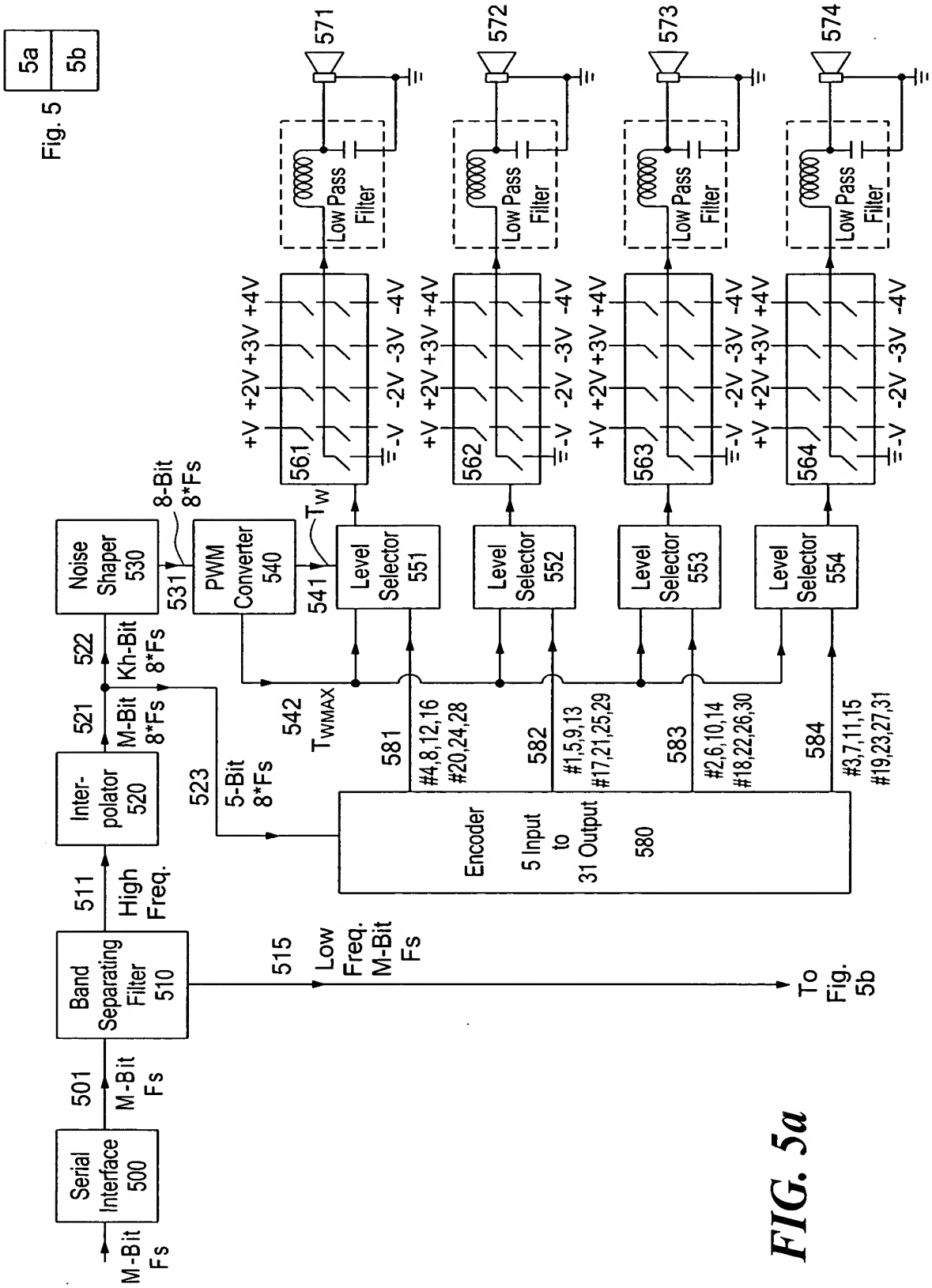

Fig. 5

5a | 5b

FIG. 5a

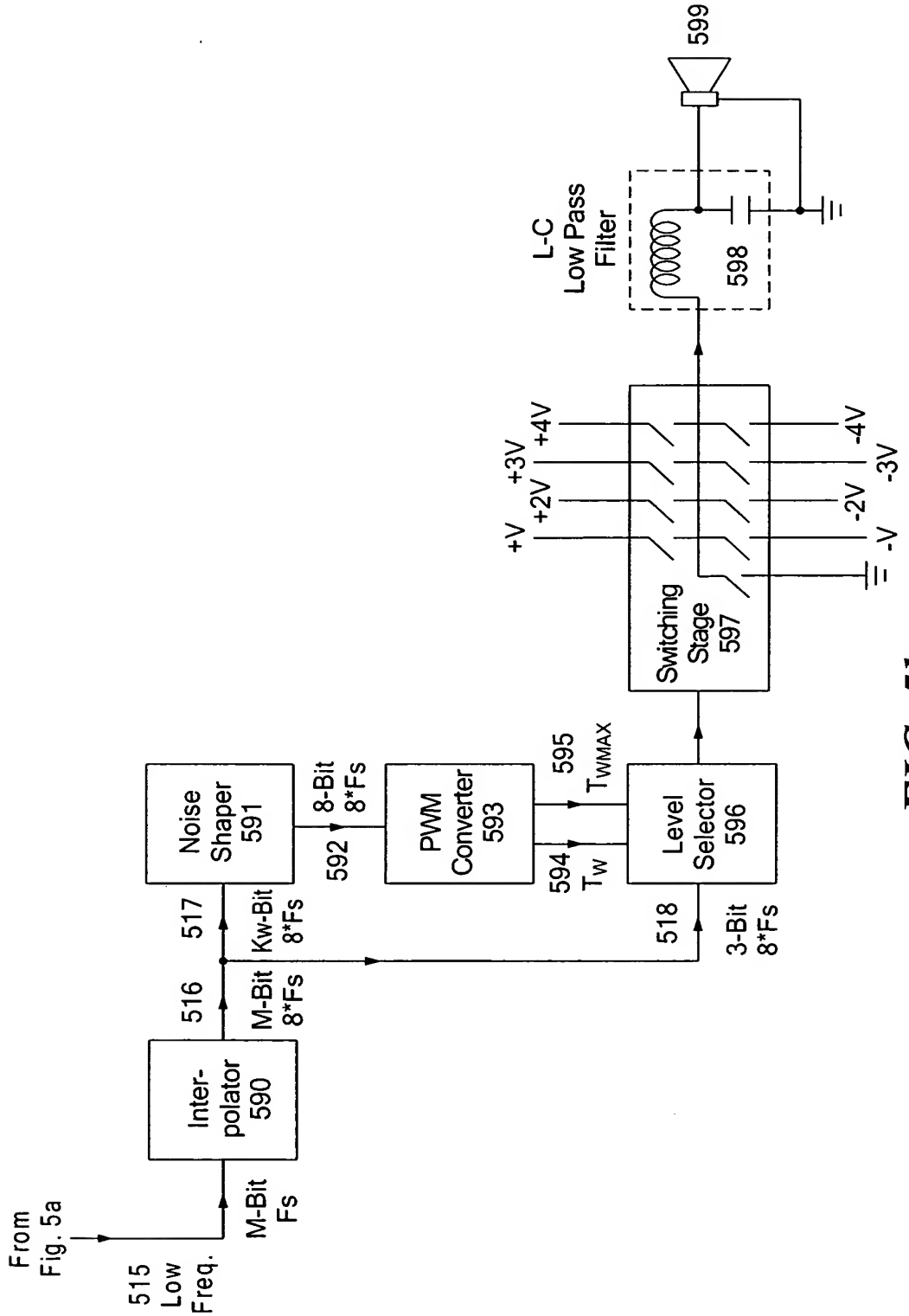
From Fig. 5a
515 Low Freq.
M-Bit Fs
Inter-polator 590
516
M-Bit 8*Fs
517
Kw-Bit 8*Fs
Noise Shaper 591
592
8-Bit 8*Fs
PWM Converter 593
594 Tw
595 TWMAX
Level Selector 596
518
3-Bit 8*Fs
Switching Stage 597
+V
+2V
+3V
+4V
-V
-2V
-3V
-4V
L-C Low Pass Filter
598
599

FIG. 5b

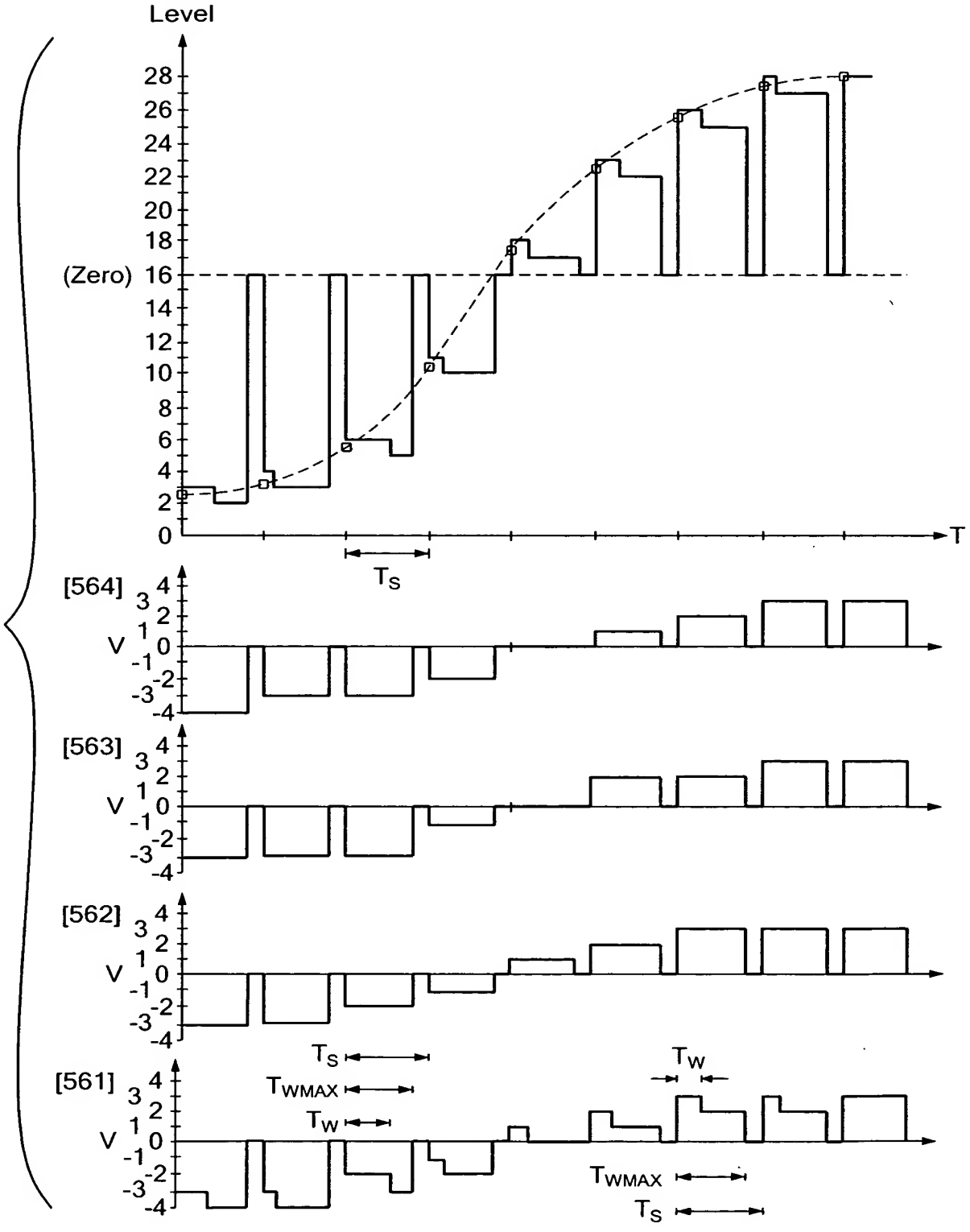
Level
28
26
24
22
20
18
(Zero) 16
14
12
10
8
6
4
2
0
T
Ts
[564]
[563]
[562]
[561]
V
Ts
TWMAX
TW
TW
TWMAX
Ts

FIG. 6